COURSE DETAILS

"CALCOLATORI ELETTRONICI"

SSD ING-INF/05

DEGREE PROGRAMME: BACHELOR DEGREE IN COMPUTER ENGINEERING

ACADEMIC YEAR: 2023-2024

GENERAL INFORMATION – TEACHER REFERENCES

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GENERAL INFORMATION ABOUT THE COURSE

INTEGRATED COURSE (IF APPLICABLE): N.A.

MODULE (IF APPLICABLE): N.A.

CHANNEL (IF APPLICABLE): N.A.

YEAR OF THE DEGREE PROGRAMME (I, II, III): I

SEMESTER (I, II): II

CFU: 9

REQUIRED PRELIMINARY COURSES (IF MENTIONED IN THE COURSE STRUCTURE "REGOLAMENTO")

None.

PREREQUISITES (IF APPLICABLE)

Basic knowledge of programming languages and fundamental algorithms to manage elementary data structures.

LEARNING GOALS

Provide methodological tools for the analysis and synthesis of elementary machines for information processing (combinatorial and sequential logical networks). Design fundamental elementary machines.
Present the fundamentals of the architecture of von Neumann electronic computers, the repertoire of operating codes and programming in assembly language.

EXPECTED LEARNING OUTCOMES (DUBLIN DESCRIPTORS)

Knowledge and understanding

The student must demonstrate knowledge and understanding of the problems related to the design of elementary machines with particular reference to elementary machines for elementary and arithmetic applications, sequential machines (registers, counters, flip flops). He must also demonstrate knowledge of the architectures of computers and their subsystems, including processor operation, how to communicate with memory, memory sizing, and connection to various input and output devices.

Applying knowledge and understanding

The student must demonstrate to be able to design and develop elementary combinatorial networks, arithmetic combinatorial networks, sequential remains.
It must also be able to develop simple assembler language programs for the management of elementary data structures (vectors, stacks,...).

COURSE CONTENT/SYLLABUS

Analysis and synthesis of combinatorial networks. Minimization of fully and incompletely specified Boolean functions. Maps of Karnaugh. Quine-McCluskey method. Synthesis of combinatorial networks in NAND and NOR logic. Delays and hazard problems in combinatorial networks.
Elementary combinatorial networks. Multiplexer and de-multiplexer. Encoder and decoder. Equality controllers. Elementary arithmetic machines: adders, subtractors, comparators.
Analysis and synthesis of sequential networks. Models for the timing and structure of synchronous and asynchronous sequential networks. Flip-flop: generalities, RS flip-flops with NOR ports. Flip-flop latch and edge-triggered. Flip-flop D. Switching flip-flop. Flip-flop T and JK. Logs. Serial and parallel loading. Scrolling registers.
Design methodology of synchronous networks. Synchronous and asynchronous counters. Connecting counters. Sequence recognizers. Bus and transfers between registers.
The electronic computer: subsystems and architecture**.**
The processor. Processor algorithm. The role of the control unit. Accumulator processors and general register processors. Addressing techniques. Encoding instructions.
The central memory. Processor-memory interface. Organization of the memory system.
Connecting memory modules. Static and dynamic RAM memories. Interconnection systems and buses. Interruption mechanism. Processor protections and controls. I/O management through polling and interruptions. The I/O subsystem.
Machine language and assembler language. Correspondence between high-level languages and machine language. Motorola 68000 processor assembler language. Assembly directives.
In-memory allocation of programs.
MC68000 processor simulator. Assembly and execution of assembler language programs. Subprograms in assembler language. Techniques for passing parameters to machine language procedures.

READINGS/BIBLIOGRAPHY

Textbooks, supplementary handouts, software tools:

G. Conte, A. Mazzeo, N. Mazzocca, P. Prinetto, "*Architettura dei calcolatori*", Città Studi Edizioni, 2015.

C. Bolchini, C. Brandolese, F. Salice, D. Sciuto, "*Reti logiche*", Apogeo Ed., 2008.

B. Fadini, N. Mazzocca, "*Reti logiche: complementi ed esercizi*", Liguori Editore, 1995.

Handouts and presentations provided by teachers related to theoretical and applicative topics covered in the course.

TEACHING METHODS

The course includes about 70% of lectures in which theoretical topics are addressed, while the remaining 30% is reserved for practical lessons and exercises concerning the development of combinatorial machines, synchronous machines and development of assembler language programs.

EXAMINATION/EVALUATION CRITERIA

a) Exam type:

The exam includes a preparatory written test that includes exercises on analysis and design of combinatorial networks, sequential networks, development of an assembler program.

Exam type	
written and oral	X
only written	
only oral	
project discussion	
other	

In case of a written exam, questions refer to:	**Multiple choice answers**	
	Open answers	X
	Numerical exercises	X

b) Evaluation pattern: